IN THE CLAIMS:

Please amend the claims as follows:

Claim 1 (Currently Amended): A method for forming a pattern over a substrate, comprising:

forming a self-aligned monolayer layer ~~resist~~ on a substrate having an etching layer thereon;

locating a master having a convex pattern over the substrate;

pressing the master against the substrate until the convex pattern of the master directly contacts the etching layer;

forming a self-aligned monolayer pattern on the etching layer exposing a portion of a surface over the substrate by separating the master from the substrate, wherein the portion of the surface has ~~removing a portion of the resist layer to expose a surface over the substrate, the removed portion of the resist layer having~~ a width substantially the same as the convex portion of the master; and

etching the etching layer using the self-aligned monolayer pattern as a mask.

Claim 2 (Original): The method of claim 1, wherein the removing a portion of the resist layer is performed by separating the master from the substrate.

Claim 3 (Original): The method of claim 1, further comprising:

forming a gate electrode and a gate line on a substrate;

forming a gate insulating layer on the gate electrode and the gate line;

forming a semiconductor layer on the gate insulating layer;

forming source/drain electrodes and a data line on the semiconductor layer; and

forming a passivation layer on the substrate.

Claim 4 (Original): The method of claim 1, wherein the resist layer is formed of a self-aligned monolayer material.

Claim 5 (Original): The method of claim 4, wherein the forming a resist layer comprises:

dissolving self-aligned monolayer molecules in ethanol;

dipping the substrate into the self-aligned monolayer molecules dissolved ethanol.

Claim 6 (Original): The method of claim 4, wherein the resist layer has a thickness of tens of angstroms (Å).

Claim 7 (Original): The method of claim 1, wherein the etching layer is an insulating layer.

Claim 8 (Original): The method of claim 6, wherein the insulating layer is one of SiOx or SiNx.

Claim 9 (Original): The method of claim 1, wherein the etching layer is a semiconductor layer.

Claim 10 (Original): The method of claim 1, wherein the etching layer is a metal layer.

Claims 11-17 (Cancelled).